REMARKS

Claims 1-12, 18 and 19 are pending in the present application. All claims were rejected in the Office Action dated August 30, 2004. Claim 1 is amended and new claims 20-23 are added. Reconsideration of all claims is respectfully requested in light of the amendments made to the claims and the arguments presented below.

Claims 1-5, 7-8, 10-11 and 18 were rejected under 35 USC 102(e) as anticipated by Chuang (U.S. Pub. No. 2004/0033663). Claim 1 as amended recites, "forming an array of first floating gate portions... subsequently forming a masking layer over areas of the substrate not covered by first floating gate portions." These limitations do not appear to be shown by Chuang. The Office Action cited "opening 207 using a mask layer 205 not covered by first floating gate portions and is self-aligned to the first floating gate portions." However, mask layer 205 does not appear to be a masking layer of claim 1. In particular, masking layer 205 does not appear to be formed subsequent to forming an array of first floating gate portions. Mask layer 205 is shown in Figure 2a of Chuang and is then removed as shown in Figures 2b. Subsequently, conductive bases 203a are formed in Figure 2g. Thus, it appears that the order of Chuang is the opposite of the order of claim 1. The conductive bases 203a appear to be formed after the mask layer 205 has already been removed.

Claims 2-12 depend from claim 1 and are therefore submitted to be allowable at least for depending from an allowable base claim. In addition, claims 2-12 contain additional claim limitations that do not appear to be shown in the prior art and are therefore submitted to be additionally allowable.

Claim 2 includes the limitation, "depositing a layer of dielectric material over the gate material, thereafter etching the dielectric material and gate material in the same pattern." This limitation does not appear to be shown by Chuang. The Office Action cited gate dielectric 202 and gate material 203 of Figure 2c as showing this feature. However, gate dielectric 202 does not appear to be "over the gate material." Gate material 203 appears to be over gate dielectric 202, which is opposite to the structure of claim 2. Therefore, these layers do not appear to have the limitations of claim 2. There does not

appear to be another dielectric layer over the layer of gate material that is etched in the same pattern as the gate material. Therefore, claim 2 is submitted to be additionally allowable.

Claim 3 includes the limitation, "implanting impurities into the substrate while first floating gate portions covered by dielectric material are present so as to implant impurities only in the areas of the substrate not covered by floating gate portions covered by dielectric material." The Office Action stated, "it is inherent that for devices in Chuang et al., source/drain regions are required and source/drain regions are formed by implanting impurities and formed into the substrate besides the gate." Even if implantation were inherent in Chuang (which is not clear) there appears to be no cited teaching of "implanting while first floating gate portions covered by dielectric material are present." Implanting, if done by Chuang, could be done at some other point. Because this limitation of claim 3 has not been shown, it is submitted that claim 3 is additionally allowable.

Claim 8 includes the limitation, "removing the sidewall elements." The Office Action cited Figure 2h of Chuang as showing this limitation. However, Figure 2h of Chuang does not appear to disclose removing spacers 208a. While spacers 208a are not shown in Figure 2h, they are clearly shown in Figure 2i, which follows Figure 2h. Also, the written description concerning Figure 2h does not appear to disclose removal of spacers 208a. It is submitted that, just because a drawing does not include a particular element, it does not mean that the element has been removed. Because there is no disclosure of removal of spacers 208 and because subsequent Figure 2i shows spacers 208a, it appears that Chuang does not remove spacers 208a. Therefore, claim 8 is submitted to be additionally allowable.

Claim 11 recites, "the conductive gates extend to enclose the second floating gate portions from above and on four lateral sides." The Office Action cited Figure 2i of Chuang as showing this limitation. However, Figure 2i of Chuang appears to be a cross-sectional view that only shows two lateral sides of elements 209a. Therefore, this does not appear to show the "four lateral sides" of claim 11 and so does not appear to anticipate this claim element. In addition, control gate 212 does not appear to enclose

protruding layer 209a on two sides in Figure 2i. Because spacer 208a extends along one lateral side of element 209a, it is not seen how control gate 212 encloses this side.

Claim 18 was rejected as anticipated by Chuang. Claim 18 recites, "forming an array of first floating gate portions, wherein each first floating gate portion is physically separated from adjacent floating gate portions, thereafter forming second floating gate portions." This limitation does not appear to be shown by Chuang. The Office action cited conductive base 203a of Chuang for the first floating gate portions and protruding layers 209a as the second floating gate portions. However, it appears that protruding layers 209a of Chuang are not formed after conductive bases 203a are formed. The first floating gate portions formed in claim 18 are "physically separated from adjacent floating gate portions." Chuang appears to show such formation in Figure 2g, which also shows elements 209a. Thus, it appears that elements 209a are formed before, or at the same time as elements 203a. The written description of Chuang, paragraphs 0034 and 0035, appears to indicate sequential formation of protruding layers 209a and conductive base 203a.

In addition, claim 18 recites, "the plane of the second floating gate portion bisects the first floating gate portion." This element of claim 18 does not appear to be shown in Figure 2g. In particular, each conductive base 203a of Chuang appears to have two protruding layers 209a. It is not clear which one is cited as bisecting conductive base 203a. It appears that the two protruding layers 209a on conductive base 203a are at either end of conductive base 203a and thus neither of these elements appear to extend along a plane that bisects conductive base 203a. Because these elements of claim 18 have not been shown in the prior art, it is requested that the rejection be withdrawn.

Claims 6, 9, 12 and 19 were rejected under 35 USC 103(a) as unpatentable over Chuang. Claims 6, 9, 12 and 19 are submitted to be allowable at least for depending from allowable base claims.

Claim 19 is submitted to be additionally allowable as containing additional limitations that are not shown in the prior art. Claim 19 recites, "the first floating gate portions are square in shape and the second portions extend from a line that is approximately a midline of the square." The Office Action noted that Chuang fails to disclose the second portion extends from approximately a midline of the first portion. It was stated that adding this element would have been obvious. However, no adequate

motivation to modify Chuang in this way was provided. Instead, it was stated, "whether the second portion of the floating gate is at midline or at one side of the first portion of the floating gate, the functions and manners of the floating gate are in this device the same." This appears to be contrary to finding a motivation to modify Chuang. If the "functions and manners" are the same, regardless of the position, this appears to imply that there is no motivation to modify Chuang by moving the second floating gate portion to a midline of the first portion. MPEP 2143.01 states, "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." Because no such indication of the desirability of modifying Chuang is provided, it is requested that the rejection be withdrawn.

In addition, the Office Action stated, "Chuang et al discloses the first portion of the floating gate is square." However, this feature has not been found in Chuang and no specific location in Chuang was provided. Therefore, it is requested that a specific reference to this element in Chuang be provided or that the rejection be withdrawn.

New claims 20-23 are added. Claims 20-23 are directed to a method of forming a non-volatile memory array and are believed to be supported throughout the specification.

Accordingly, it is believed that all claims are in condition for allowance and an indication of their allowance is requested. However, if the Examiner is aware of any additional matters that should be discussed, a call to the undersigned attorney at: (415) 318-1160 would be appreciated.

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 30, 2004.

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Respectfully submitted,

Gerald P. Parsons — Date 11/30/04
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